REMARKS

Claims 25-31 and 44-46 are pending in the present application. Claims 25-32 and 44-47 were examined. Claims 32 and 47 have been cancelled by amendment.

In the office action mailed November 29, 2005 (the "Office Action"), the Examiner rejected claims 25, 27, 29, 30, 32, 44, 46, and 47 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,124,660 to Cilingiroglu (the "Cilingiroglu patent") in view of U.S. Patent No. 6,097,203 to Parker *et al.* (the "Parker patent"). The Examiner also rejected claim 26, 28, 31, and 45 under 35 U.S.C. 103(a) as being unpatentable over the Cilingiroglu patent in view of the Parker patent, and further in view of U.S. Patent No. 6,242,941 to Vest *et al.* (the "Vest patent") and U.S. Patent No. 6,714,031 to Seki (the Seki patent").

As previously mentioned, the Examiner has rejected claims 25, 27, 29, 30, 32, 44, 46, and 47 under 35 U.S.C. 103(a) as being unpatentable over the Cilingiroglu patent in view of the Parker patent. In formulating the rejection of the claims, the Examiner acknowledges that the Cilingiroglu patent fails to teach or suggest a test plate integrated in the integrated circuit. However, the Parker patent makes up for this deficiency by teaching "a test plate integrated in the integrated circuit for enabling continuity testing the package or integrated circuit." *See* the Office Action at page 2.

The Parker patent describes various embodiments of integrated structures and circuits that can be used to test electrical continuity between bond pads of an integrated circuit ("IC") and an electrical trace on a substrate, such as a printed circuit board. In one embodiment, internal conductive pads 308 are integrated as part of IC 300 for use as capacitive test probes for testing the continuity between bonding pads 302 and traces on substrate 312. *See* Figure 3A and col. 7, lines 17-32. The internal conductive pads 308 can be used in place of capacitive probe 132 in the arrangement for testing electrical continuity as illustrated in Figure 1 of the Parker patent. As with the technique for testing continuity described in the Cilingiroglu patent (see remarks from previously filed response for a description) and described in the Parker patent at col. 4, lines 30-55, an alternating voltage is applied to either the capacitive probe or electrical trace and an induced current is measured. Based on the magnitude of the induced current, a determination is made whether there is electrical continuity or not. The Parker patent further discloses other embodiments for continuity testing that utilize integrated capacitive probes

(Figure 3A, 3B, 6A, and 6B), Hall-effect probes (Figures 4A and 4B) and conductive loops (Figures 5 and 7).

Claims 25 and 44 are patentable because neither the Cilingiroglu or the Parker patent, individually or in combination, teach or suggest the combination of limitations recited by claims 25 or 44. For example, neither the Cilingiroglu or Parker patents teach or suggest using an integrated test plate capacitively coupled to data terminals for testing the receipt of data signals through a capacitive medium. Unlike the continuity testing that is described in both the Cilingiroglu and Parker patents, signals encoded with data are applied to the test plate to be transmitted to the data terminals in various embodiments of the present invention. As described in the Cilingiroglu and Parker patents, an alternating voltage is applied to the electrode capacitively coupled to the terminals of the IC, or to the terminals themselves, and the induced current is measured. The alternating voltage does not represent data or any information, which is consistent with the purpose of determining electrical continuity as described in both the Cilingiroglu and Parker patents. In contrast, the claimed inventions of the present application specifically recite that data signals representing test data are applied to the integrated test plate to be transmitted to the data terminals. Internal data signals are generated in response to receiving the transmitted data signals. Data represented by the internal data signals are then compared with the test data to determine whether there are any discrepancies between the transmitted and received data. If there are discrepancies, this suggests that the device may be defective.

Testing for data integrity as previously described is generally embodied by the language of the claims. For example, claim 25 recites a method of evaluating an integrated circuit that includes transmitting a data signal representing expected data from a test plate that is capacitively coupled to a plurality of test terminals. The data signal is received by at least one of the plurality of data terminals and an internal data signal representing received data is generated in response to receipt of the data signal at the data terminal. The received data represented by the internal data signal is then compared to the expected data represented by the data signals. Similarly, claim 44 recites a test apparatus for an integrated circuit that includes a test transmitter circuit coupled to a test plate integrated in the integrated circuit. The test transmitter circuit is configured to apply a test data signal to the test plate that is transmitted to at least one of the signal terminals as an input data signal. The test data signal represents expected data. The test apparatus further includes a test unit coupled to the integrated circuit that is configured to

compare received data represented by the received data signal to the expected data represented by the test data signal. In both claims 25 and 44, data signals are applied to and transmitted by the test plate. The data represented by the data signals received by the data terminals is then compared to the expected data of the transmitted data signals to determine whether the data was successfully received.

As previously described, neither the Cilingiroglu or Parker patents, individually or in combination, teach or suggest testing the receipt of data signals by the data terminals that have been transmitted by a test plate capacitively coupled to the data terminals. The Cilingiroglu and Parker patents are directed to techniques for determining electrical continuity by means of capacitive coupling and induced currents. For the foregoing reasons, claims 25 and 44 are patentable over the Cilingiroglu patent in view of the Parker patent. Claims 27, 29, and 30, which depend from claim 25, and claim 46, which depends from claim 44, are similarly patentable based on their dependency from a respective allowable base claims. Therefore, the rejection of claims 25, 27, 29, 30, 44, and 46 under 35 U.S.C. 103(a) should be withdrawn.

As previously mentioned, the Examiner rejected claims 26, 28, and 31 under 35 U.S.C. 103(a) as being unpatentable over the Cilingiroglu patent in view of the Parker patent, and further in view of the Vest patent. The Examiner also rejected claim 45 under 35 U.S.C. 103(a) as being unpatentable over the Cilingiroglu patent in view of the Parker patent, and further in view of the Seki patent.

The Examiner has cited the Vest patent as teaching placing terminals in a high-impedance state for reducing noise while in a test mode and has cited the Seki patent as teaching a test transmitter comprising a buffer circuit. *See* the Office Action at page 4 and 5. Even if the Examiner's characterizations of the Vest and Seki patent are assumed to be accurate, neither reference makes up for the deficiencies of the combined teachings of the Cilingiroglu and Parker patents previously discussed with respect to claims 25, 27, 29, 30, 44, and 46. For the foregoing reasons, claims 26, 28, 31, and 45 are patentable over the Cilingiroglu patent in view of the Parker patent, and further in view of either the Vest or Seki patents.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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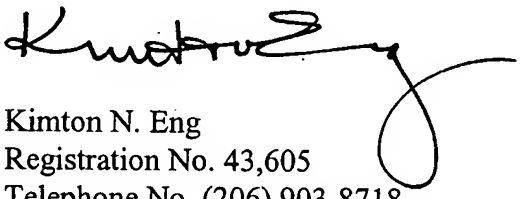

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